Advanced Digital Design - EENG484

https://coulston.github.io/Advanced-Digital-Design/index.html

Fall 2025

Dr. Chris Coulston, Teaching Professor, 303.273.3265, coulston@mines.edu

Office: BB 310E (Brown Hall)
Office hours: MWF 9:00 – 9:50
Course Title: Advanced Digital Design

Course Meeting: Lecture MWF 9:00-9:50 204 Hill Hall

Course Description: Explore hardware/software co-design by designing a data acquisition system in VHDL and interfacing it to a general purpose processor.

Textbook(s):

None, class notes will be provided through the term.

Course Objectives:

Design and build a data acquisition and control systems. In order to accomplish this, there are detailed objectives for specific topics:

- 1. Design and implement a complex, structured, synthesizable digital system that meets defined requirements.
- 2. Use contemporary software tools to debug a digital system design and verify that a digital system meets defined requirements.
- 3. Analyze and describe the timing, clock, and synchronization requirements for a given digital system.
- 4. Design and implement a digital system using a fully custom-built hardware solution, interfaced to a general-purpose processor.
- 5. Explore hardware/software co-design.

Lab: We will work in the classroom and in 304/305 Brown Hall.

Office Hours: I like to pile everyone in my office during office hours. What this means is I generally like to have everybody in the office asking questions. In this way, many problems can be addressed at once. Since I teach multiple classes, there may be students from a different class all piled in my office. If this is the case, please interrupt me and let me know that you have a question from a different class. I will let the students present know that I need to attend to a question from another class and give them and give them 10 minutes to wrapup their questions before I switch to yours.

Computers: We will be working with computers throughout this semester. Inevitably there will be problems that you will encounter. If a computer or its software is malfunctioning, then please report it. I want you to deal with HW/SW problems in a manner conducive to engineering students, deal with the lab staff in an objective and rational manner. The computer center staff works hard to keep our problems to a minimum. Establishing a positive relationship with them will help expedite solutions to any problems we may have. If there are major problems with the system during critical times, I will be made aware of them and will determine an appropriate course of action.

Topics Covered: See the main course web page for a timeline; changes may be made through the semester.

Session	Date	Topic	Due
1	Aug 25 (M)	Symbolic to VHDL, entity architecture, std_logic, signals	243
2	Aug 27	TT to VHDL, Literals, Vectors, Don't cares	Homework 1
3	Aug 29	Generics, Basic Building Block, Entity and Architecture	Homework 2
	Sept 1 (M)	Labor Day	
4	Sept 3	Sequential Building Blocks	Homework 3
5	Sept 5	Libraries, Testbench	Homework 4
6	Sept 8 (M)	Design of enhanced PWM	
7	Sept 10	Lab Day – Enhanced PWM	
8	Sept 12	Lab Day – Enhanced PWM Lab Due	
9	Sept 15 (M)	VHDL Synthesis - Porting PWM to PL in Zynq	
	Sept 17	Career Day	
10	Sept 19	VGA Standard	Homework 5
11	Sept 22 (M)	Design of VGA to HDMI	TIGHTOWORK 0
12	Sept 24	Lab Day – VGA to HDMI	
13	Sept 26	Lab Day – VGA to HDMI	
14	Sept 29 (M)	Lab Day – VGA to HDMI	Lab Due
15	Oct 1	Datapath and control architecture and timing	Lub Duo
16	Oct 3	Stopwatch Control Unit in VHDL	Homework 6
17	Oct 6 (M)	Stopwatch Datapath in VHDL	Homework 7
18	Oct 8	Exam Review	Homework 8
19	Oct 10	Exam	Tielliewerk e
20	Oct 13 (M)	AD7606 chip, Input, Output and Behavior	
21	Oct 15	Design of datapath and control for acquire	
22	Oct 17	Design of datapath and control for acquire	
	Oct 20 (M)	Fall Break	
23	Oct 22	Lab Day – Acquire	
24	Oct 24	Lab Day – Acquire	
25	Oct 27 (M)	Lab Day – Acquire	Lab Due
26	Oct 29	BRAM, IP I/O and Behavior	245 245
27	Oct 31	Design of datapath and control for acquire to display	
28	Nov 3 (M)	Design of datapath and control for acquire to display	
29	Nov 5	Lab Day – Acquire to display	
30	Nov 7	Lab Day – Acquire to display	
31	Nov 10 (M)	Lab Day – Acquire to display	Lab Due
32	Nov 12	Building Custom IP	
33	Nov 14	Programming Custom IP	
34	Nov 17 (M)	Lab Day – Enhanced PWM with Zyng	
35	Nov 19	Lab Day – Enhanced PWM with Zynq	
36	Nov 21	Lab Day – Enhanced PWM with Zynq	Lab Due
	Nov 24 – 28	Thanksgiving	
37	Dec 1 (M)	Design of acquire to HDMI	
38	Dec 3	Lab Day – Acquire to HDMI	
39	Dec 5	Lab Day – Acquire to HDMI	
40	Dec 8 (M)	Lab Day – Acquire to HDMI	
41	Dec 10	Lab Day – Acquire to HDMI	Lab Due
		, , , , , , , , , , , , , , , , , , ,	

Programs: Programming assignments will be evaluated using the rubric posted by the instructor or lab assistants during the class period which it is due. Your code will be evaluated on style and functionality.

- **Style** is a subjective measure which evaluates how effectively the solution was arrived at. The following are attributes which constitute good style practices.
 - o Minimizing the amount of code (within reason).
 - o Minimizing the amount of data storage (within reason).
 - Approach the problem in an obvious manner.
 - o Breaking the problem into logical subcomponents.
 - o Consistently use all upper-case letters for constants (#define's and constants).
 - Consistently use camel case for signals.

- Consistently use camel case for entity names and the names of instanced. Any additional description of the entity or instance's name should be separated by an underline. For example, acquireToHdmi_datapath.
- o Using libraries to hold entity descriptions and constants.
- Use named association of signal assignment in component instantiation, do not use positional association. Put one signal on each line and use open to declare unconnected signals.
- **Functionality** You will be asked to demonstrate that your program meets the functional requirements posted in the lab assignment.

Exams:

- Exams will be scheduled during the class meeting time,
- Exams will be administrated in person,
- The academic integrity guidelines apply while you are taking the exam.

Makeup Exams: Makeup exams can be arranged. Prior arrangements are appreciated but if some major emergency should arise and you cannot make it to an exam it is your responsibility to:

- 1. Contact me at my office phone (303.273.3265), or
- 2. Contact me by email (coulston@mines.edu).

Contact me as soon as you are able to return to campus. In general, I am pretty understanding about makeup exams – I do not want anyone hurt attempting to make it to campus as a result of foul weather. Please show me the same respect as you would like me to show you in complying with these guidelines.

Homework: Throughout the term I will administrate homework to test your understanding of material presented during lecture. Your lowest two quizzes will be dropped from your final grade. No late homework will be accepted.

Grades: The grade you earn in this class will be based on the following distribution of points:

Exam 1	20%
Labs	50%
Final Proj.	20%
Homework	10%

Grade	Upper	Lower
Α	100	93+
A-	93-	90+
B+	90-	87+
В	87-	83+
B-	83-	+08
C+	80-	77+
С	77-	73+
Ċ	73-	70+
D+	70-	63+
D	67-	63+
D-	63-	60+
F	60-	0.0

Academic Integrity: The Colorado School of Mines affirms the principle that all individuals associated with the Mines academic community have a responsibility for establishing, maintaining and fostering an understanding and appreciation for academic integrity. In broad terms, this implies protecting the environment of mutual trust within which scholarly exchange occurs, supporting the ability of the faculty to fairly and effectively evaluate every student's academic achievements, and giving credence to the university's educational mission, its scholarly objectives and the substance of the degrees it awards. The protection of

academic integrity requires there to be clear and consistent standards, as well as confrontation and sanctions when individuals violate those standards. The Colorado School of Mines desires an environment free of any and all forms of academic misconduct and expects students to act with integrity at all times. Academic misconduct is the intentional act of fraud, in which an individual seeks to claim credit for the work and efforts of another without authorization, or uses unauthorized materials or fabricated information in any academic exercise. Student Academic Misconduct arises when a student violates the principle of academic integrity. Such behavior erodes mutual trust, distorts the fair evaluation of academic achievements, violates the ethical code of behavior upon which education and scholarship rest, and undermines the credibility of the university. Because of the serious institutional and individual ramifications, student misconduct arising from violations of academic integrity is not tolerated at Mines. If a student is found to have engaged in such misconduct sanctions such as change of a grade, loss of institutional privileges, or academic suspension or dismissal may be imposed. For this course, the following rules should be followed.

- Copying of solutions without understanding them is not allowed; if a student copies a solution and cannot explain it adequately this is considered academic dishonesty.
- During quizzes and exams, students must do 100 percent of the work on their own.
- The nominal penalty for academic dishonesty is an 'F' in the course.

Disability Support Statement:

The Colorado School of Mines is committed to ensuring the full participation of all students in its programs, including students with disabilities. If you are registered with Disability Support Services (DSS) and I have received your letter of accommodation, please contact me at your earliest convenience so we can discuss your needs in this course. For questions or other inquiries regarding disabilities, I encourage you to visit disabilities.mines.edu for more information.

Absenteeism (from Undergraduate Bulletin)

Class attendance is required of all undergraduates unless the student has an official excused absence. Excused absences are granted for three general reasons:

- 1. Student is a varsity athlete and is representing the school in a varsity athletics activity.
- 2. Student is representing the school in an authorized activity related to a club or academic endeavor (academic competitions, student professional society conferences, club sport competition, program-sponsored competitions, etc.)
- 3. Student has a documented personal reason (illness, injury, jury duty, life-threatening illness or death in the immediate family, military service, etc.).

Students who miss academic work (including but not limited to exams, homework, and labs) for one of the reasons listed above may be issued an excused absence. If an excused absence is received, the student must be given the opportunity to make up the missed work in a reasonable period of time without penalty. While the student is not responsible for actually issuing the excused absence, the student is responsible for making sure documentation is submitted appropriately and for contacting his/her faculty member(s) to initiate arrangements for making up any missed work.